GAU 2761

O I E JC51
NOV 3 0 1998
PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NO.: S1022/8126

#2
12/4/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Geoff BARRETT
Serial No.: 09/159,748
Filing Date: September 23, 1998
For: APPARATUS FOR PROVING SYSTEM PROPERTIES

RECEIVED
DEC 0 3 1998
Group 2700

Examiner: Unassigned
Art Unit: 2761

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Certified Copy of United Kingdom Priority Application No. 9720648.6
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

A check in the amount of $0.00 is enclosed to cover the filing fee. If the fee is insufficient, the balance may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on November 24, 1998.

Attorney Docket No.: S1022/8126

XNDD

Respectfully submitted,

James H. Morris
Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

This [illegible] [illegible]ank (u[illegible]

This Page Blank (usp[illegible]

PE JC51
NOV 30 1998
PATENT & TRADEMARK OFFICE

The Patent Office

The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP9 1RH

RECEIVED

DEC 03 1998

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., [illegible] L.C. or PLC.

[illegible]istration under the Companies Act does not constitute a new legal entity but merely [illegible]s the company to certain additional company law rules.

Signed [signature]

Dated 28.10.98

Patents Form 1/77

Patents Act 1977
(Rule 16)

THE PATENT OFFICE
29 SEP 1997
RECEIVED BY HAND

The Patent Office

29 SEP 1997

The Patent Office
Cardiff Road
Newport
Gwent NP9 1RH

30SEP97 E306408-1 D00068
P01/7700 25.00 - 9720648.6

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

1.	Your reference	83839/WJN
2.	Patent application number *(The Patent Office will fill in this part)*	9720648.6
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	SGS-THOMSON MICROELECTRONICS., LTD. Planar House, Parkway, Globe Park, Marlow, Bucks SL7 1YL
	Patents ADP number *(if you know it)*	
	If the applicant is a corporate body, give the country/state of its incorporation	United Kingdom C422 773 001
4.	Title of the invention	METHOD AND APPARATUS FOR PROVING SYSTEM PROPERTIES 29 SEP 1997
5.	Name of your agent *(if you have one)*	Page White & Farrer
	"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	54 Doughty Street London WC1N 2LS
	Patents ADP number *(if you know it)*	1255003

		Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	None		

		Number of earlier application	Date of filing *(day / month / year)*
7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application		

8.	Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:* *a) any applicant named in part 3 is not an inventor, or* *b) there is an inventor who is not named as an applicant, or* *c) any named applicant is a corporate body* *See note (d))*	Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	0
Description	9
Claim(s)	3
Abstract	0
Drawing(s)	4

10. If you are also filing any of the following, state how many against each item.

Priority documents	N/R
Translations of priority documents	N/R
Statement of inventorship and right to grant of a patent (Patents Form 7/77)	0
Request for preliminary examination and search (Patents Form 9/77)	0
Request for substantive examination (Patents Form 10/77)	0
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature

Date 29.09.97

12. Name and daytime telephone number of person to contact in the United Kingdom — W J Neobard 0171-831-7929

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

a) *If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.*

b) *Write your answers in capital letters using black ink or you may type them.*

c) *If there is not enough space for all the relevant details on any part of this form. please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.*

d) *If you have answered 'Yes' Patents Form 7/77 will need to be filed.*

e) *Once you have filled in the form you must remember to sign and date it.*

f) *For details of the fee and ways to pay please contact the Patent Office.*

METHOD AND APPARATUS FOR PROVING SYSTEM PROPERTIES

The present invention relates to a method and apparatus for reducing the complexity of a representation of a hardware system.

The first stage in synthesizing and proving the properties of a system is a compilation process in which the system is represented as a set of functions comprising:-

a first subset of functions which determines the value of system outputs as a function of system inputs, system states represented by state bits, and internal signals;

a second subset of functions which determines the values of state bits on the next clock cycle as a function of system inputs, system states represented by state bits, and internal signals; and

a third subset of functions which determines the values of internal signals as a function of system inputs, system states, and internal signals.

To enable or accelerate formal proof, internal signals may be eliminated from the system model by substituting them into the functions which refer to them. In the course of this substitution, the representation of the model may become extremely large. If this occurs, it is possible to detect an explosion in the size of the representation and to suspend the substitution process while restructuring the representation to seek a reduction in size.

Typically in a compilation process static relationships between signals in the system model can be destroyed by dynamic restructuring operations. This can lead to a further explosion later during the substitution process.

It would be advantageous to take static relationships into account during the dynamic restructuring process.

One technique of representing functions and internal signals

is by the use of binary decision diagrams (BDD's). A binary decision diagram is a representation of a digital function which contains the information necessary to implement the function. The diagram is a tree-like structure having a root and plural nodes, where the root represents the digital function and the nodes are labelled with variables. Each node has two branches, one representing the assertion that the variable labelling the node is 1, and the other representing the assertion that the variable labelling the node is 0. In a BDD, "ordering" relates to the order in which variable names are encountered during traversal of the graph. Better orderings result in fewer nodes in the graph.

According to a first aspect of the present invention, there is provided a method for selecting an order in which to sift variables in a binary decision diagram comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variable of the system such that the set of functions labelling leaves reachable from a node, correspond to the set of functions which depend on the variables labelling the nodes; and

traversing the graph in a depth first manner, thereby to produce a list of said labels in said selected order.

According to a second aspect of the present invention there is provided apparatus for selecting an order in which to sift variables in a binary decision diagram comprising a first store storing bits representing the variables of a binary decision diagram;

a second store and processor means;

wherein said processor means arranges the said variables of said binary decision diagram in a representation of the nodes of a graph in which the nodes are labelled with the variables such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

means for traversing the graph in a depth-first manner such

that said processor means outputs to said second store a list of said labels in said selected order.

According to a third aspect of the present invention there is provided a method for restructuring a binary decision diagram representative of a hardware system, comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

Preferably said variables are sifted one-by-one to a deepest best location. Advantageously said variables are sifted one-by-one in said selected order to a deepest best location followed by sifting in reverse order to a shallowest best location.

According to a fourth aspect of the present invention there is provided apparatus for restructuring a binary decision diagram comprising:-

storage means for storing bits representative of a set of functions as binary decision diagrams having a plurality of nodes labelled by variables;

processor means for detecting a number of nodes of said binary decision diagram, and in response to such detection, arranging the variables of said binary decision diagram on the nodes of a graph in which the nodes are labelled such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in a selected order and using said selected order, controlling sifting of variables of said binary decision diagrams;

wherein said sifted binary decision diagram is written by said processor means to said storage means.

According to a fifth aspect of the present invention there is provided a method for proving the properties of a hardware system comprising:-

representing said system as binary decision diagrams having a plurality of nodes labelled by variables;

substituting functions which determine variables of internal signals;

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

According to a sixth aspect of the present invention there is provided apparatus for proving the properties of a hardware system comprising:

storage means for storing bits representative of a set of functions which represent the hardware system as binary decision diagrams having a plurality of nodes labelled by variables;

processor means for substituting functions which determine the values of internal signals into the set of functions representing said system and detecting an increase in the number of nodes of said binary decision diagram, and, in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponding to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in said selected order, and using said selected order

controlling sifting of the variables of said binary decision diagram; and

further comprising a second store, wherein said sifting binary decision diagram is written by said processor to said second store.

Preferably said number is a threshold derived from an original number of nodes.

Alternatively said number of nodes is the number of nodes which branches on a predetermined variable.

Alternatively said number is an absolute number.

An embodiment of the present invention will now be described with respect to the following drawings in which:-

Figure 1 shows a binary decision diagram for the function

$$f = x \text{ OR } y;$$

Figure 2 shows a logical diagram of a multiplexer;

Figure 3 shows a binary decision diagram for the equation;

$$b_i = \text{NOT } (a_i \text{ AND } s_i);$$

Figure 4 shows the binary decision diagram for the equation

$$d = \text{NOT } (b_1 \text{ AND } b_2 \text{ AND } b_3 \ldots b_n);$$

Figure 5 is an optimally ordered substitution of the equations of Figures 3 and 4; and

Figure 6 shows a graph of relationships between the variables of the multiplexer of Figure 2.

A Binary Decision Diagram (hereinafter referred to as a BBD) is a directed acyclic graph representative of a Boolean function as a decision procedure based on the variables on which it

depends. For instance, for the function:-

f = x OR y,

f can be implemented by the decision procedure "if x then true else if y then true else false". Each of the "if...then...else..." constructs of this decision procedure can be represented as a node in a graph.

Referring to Figure 1, the first node 1 is labelled with the variable x and there are two branches from this first node, one 11 is "true" and the other 12 is "if y then true else false". This other branch 12 leads to a second node 2 which is labelled with the variable y, which in turn has two branches 21, 22 of which one is "true" and the other is "false".

It will be understood that although the nodes 1 and 2 are described above as being labelled with <u>variables</u>, nevertheless these labels could in fact refer to functions which upon evaluation would give rise to the logical values "true" or "false".

Referring now to Figure 2, a multiplexer consists of a first set of n NAND gates 10_1-10_n, each gate having two respective inputs a_1-a_n, s_1-s_n. The outputs lines b_1 and b_n of the gates are connected to an n-input NAND gate 20 having an output d.

Thus, in terms of a system as described in the preamble to this patent application, the multiplexer of Figure 2 has system inputs (a_1-a_n, s_1-s_n), internal signals (b_1-b_n) and a system output (d). The output d is related to the internal signals b_1-b_n by the equation:-

$$d = \text{NOT } (b_1 \text{ AND } b_2 \text{ AND } b_3 \ldots b_n)$$

and each internal signal b_i to the respective inputs a_i and s_i by the equation

$$b_i = \text{NOT } (a_i \text{ AND } s_i)$$

Thus,

$$d = (a_1 \text{ AND } s_1) \text{ OR } (a_2 \text{ AND } s_2) \text{ OR} \ldots (a_n \text{ AND } s_n)$$

Referring to Figure 3 the relationship b_i = NOT (a_i AND s_i) is shown as a binary decision diagram.

Figure 4 shows the binary decision diagram representation of the expression for d in terms of the internal signals b.

By inspection, there are 3n variables (a_i, s_i and b_i) and there are thus (3n)! apparently equally good orderings possible. However, by inspection of the overall equation for the device it would be seen that a_1 and s_1 are associated together, a_2 and s_2 are associated together and so on which means that there are in fact only n! orderings which are optimal for the entire system.

An advantage of the present invention is that it enables more information about the system as a whole to be taken into account when performing operations which would otherwise <u>not</u> take this information into account. Failing to take the information into account can result in following paths which do not lead to a solution, or which are highly inefficient in reaching the solution.

Figure 5 shows a binary decision diagram for the multiplexer of Figure 2 in which the respective pairs of inputs are associated together.

The size of a binary decision diagram is sensitive to the order in which the variables are inspected, and efficient BDD reordering is very important. One algorithm for reordering is "sifting", wherein each variable is taken in turn and the best position of it is found by trying it in every possible position of the BDD. It is then necessary to decide which variable to take first. A known and frequently successful tool for doing this is to rank the variables according to which variable labels the

greatest number of nodes and then to sift in the order of ranking.

In the present BDD, it is clear that each variable labels a single node and thus it would not be possible using known techniques to identify a highest ranking variable. Conventionally, in such a situation, an arbitrary order for sifting would be used.

The present invention makes use of a function graph which is traversed to determine an order for sifting.

As used herein, a function graph is a directed acyclic graph where the leaves are labelled with functions and the nodes are labelled with sets of variables (non-empty). The only restriction put on this graph is that a variable which is in the set labelling a node is in the "cone" of all the functions at the leaves below it and no others. This restriction plus the fact that the sets of variables must be non-empty, is enough to ensure that the graph is unique. The "cone" of a function is herein defined to be all those variables on which a function depends, either directly or through the intermediate signals on which it depends.

Using a function graph to define an ordering of the variables in a BDD to minimise its size may be related to the register allocation technique used in software compilation in that the ordering of the variables is derived from a traversal of the function graph in such a way that no node is visited before all of its predecessors has been visited, but each node is visited as soon as all its predecessors have been visited, unless there is a race between more than one node, in which case one of the competing nodes is chosen and its subgraphs traversed first.

Figure 6 shows a function graph for the multiplexer of Figure 2 having a root labelled by b_1-b_n intermediate nodes

labelled by a_1, s_1, a_2, $s_2 \ldots a_n$ s_n and leaves as shown. Traversing this function graph from the top down gives the order:-

$b_1, b_2 \ldots b_n, a_1, s_1, a_2, s_2 \ldots . a_n, s_n$

By using this order which is derived from static information of the system, the binary decision diagrams of (in this case) Figures 1, 3 and 4 are sifted to provide an optimal order. This order is that represented by Figure 5.

It should be noted that substitution may be effected without restructuring the BDD, while monitoring the size of the BDD. If an explosion in BDD size is detected, sifting is then effected on the basis of the order provided by the present invention.

CLAIMS:-

1. A method for selecting an order in which to sift variables in a binary decision diagram comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variable of the system such that the set of functions labelling leaves reachable from a node, correspond to the set of functions which depend on the variables labelling the nodes; and

traversing the graph in a depth first manner, thereby to produce a list of said labels in said selected order.

2. Apparatus for selecting an order in which to sift variables in a binary decision diagram comprising a first store storing bits representing the variables of a binary decision diagram;

a second store and processor means;

wherein said processor means arranges the said variables of said binary decision diagram in a representation of the nodes of a graph in which the nodes are labelled with the variables such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

means for traversing the graph in a depth-first manner such that said processor means outputs to said second store a list of said labels in said selected order.

3. A method for restructuring a binary decision diagram representative of a hardware system, comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

4. A method as claimed in claim 3 wherein said variables are sifted one-by-one to a deepest best location.

5. A method as claimed in claim 3 wherein said variables are sifted one-by-one is said selected order to a deepest best location followed by sifting in reverse order to a shallowest best location.

6. Apparatus for restructuring a binary decision diagram comprising:-

storage means for storing bits representative of a set of functions as binary decision diagrams having a plurality of nodes labelled by variables;

processor means for detecting a number of nodes of said binary decision diagram, and in response to such detection, arranging the variables of said binary decision diagram on the nodes of a graph in which the nodes are labelled such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in a selected order and using said selected order, controlling sifting of variables of said binary decision diagrams;

wherein said sifted binary decision diagram is written by said processor means to said storage means.

7. A method for proving the properties of a hardware system comprising:-

representing said system as binary decision diagrams having a plurality of nodes labelled by variables;

substituting functions which determine variables of internal signals;

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

8. Apparatus for proving the properties of a hardware system comprising:

storage means for storing bits representative of a set of functions which represent the hardware system as binary decision diagrams having a plurality of nodes labelled by variables;

processor means for substituting functions which determine the values of internal signals into the set of functions representing said system and detecting an increase in the number of nodes of said binary decision diagram, and, in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponding to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in said selected order, and using said selected order controlling sifting of the variables of said binary decision diagram; and

further comprising a second store, wherein said sifting binary decision diagram is written by said processor to said second store.

9. Apparatus as claimed in claim 8 wherein said number is a threshold derived from an original number of nodes.

10. Apparatus as claimed in claim 8 wherein said number of nodes is the number of nodes which branches on a predetermined variable.

11. Apparatus claimed in claim 8 wherein said number is an absolute number.

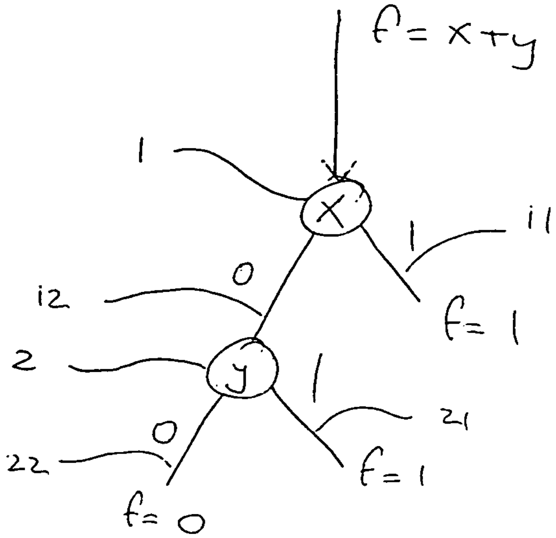
f = x + y
1
x
11
1
0
12
f = 1
2
y
1
21
0
22
f = 1
f = 0

Fig 1

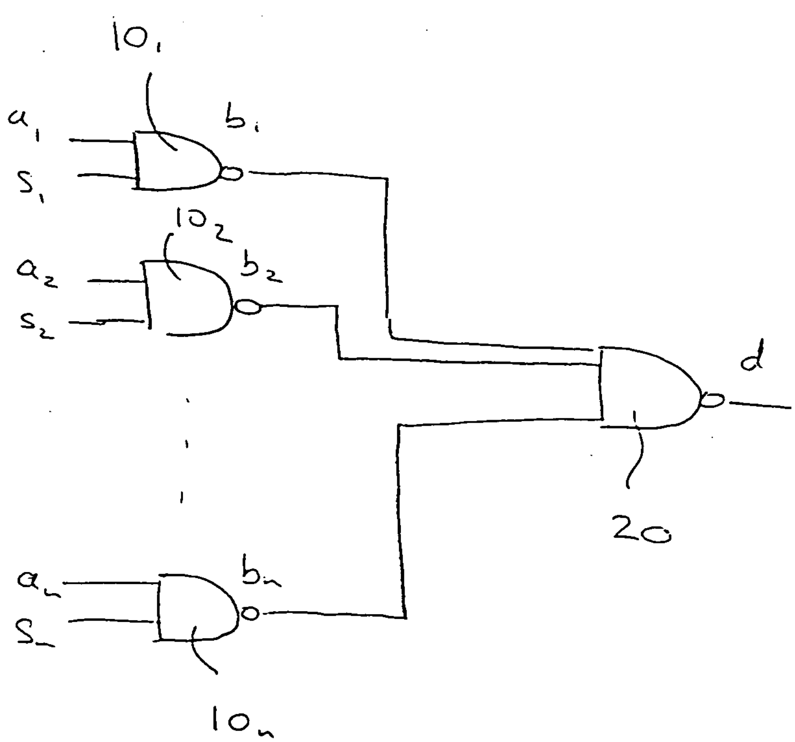
10₁
a₁
b₁
s₁
10₂
a₂
b₂
s₂
d
20
aₙ
bₙ
sₙ
10ₙ

FIG 2

$$b_i = \overline{a_i \cdot s_i}$$

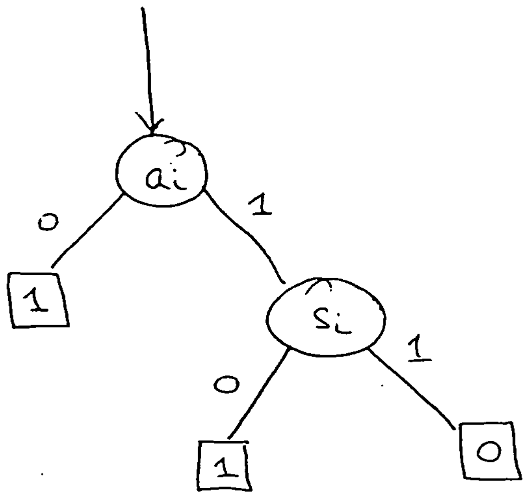

FIG 3

$$d = \overline{b_1 \cdot b_2 \cdots b_n}$$

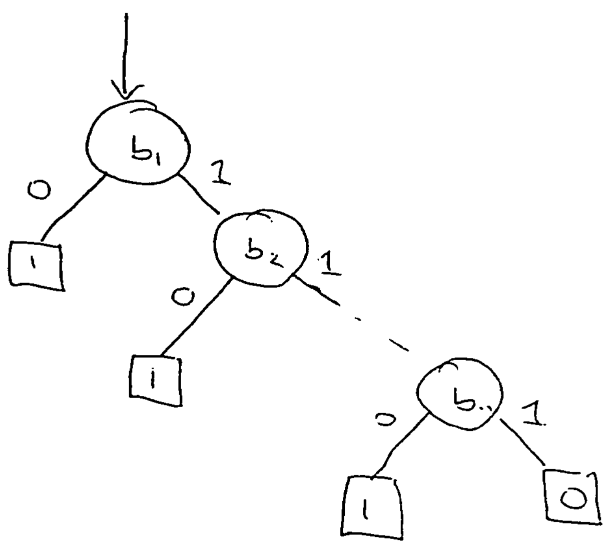

FIG 4

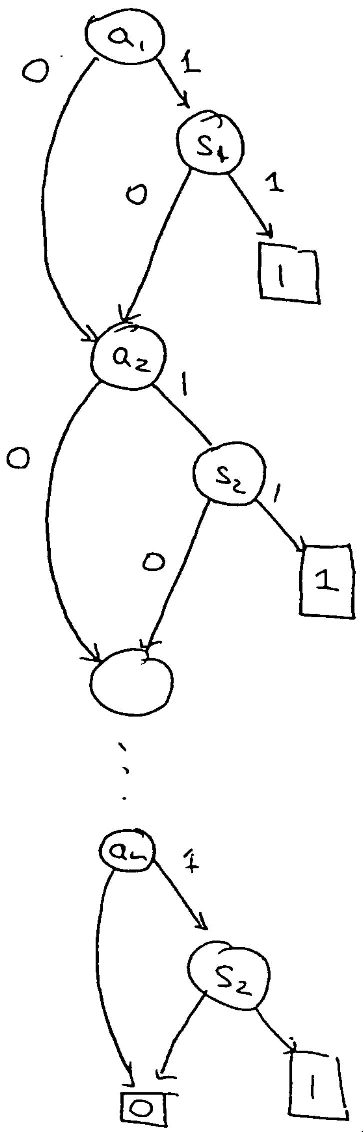

FIG 5

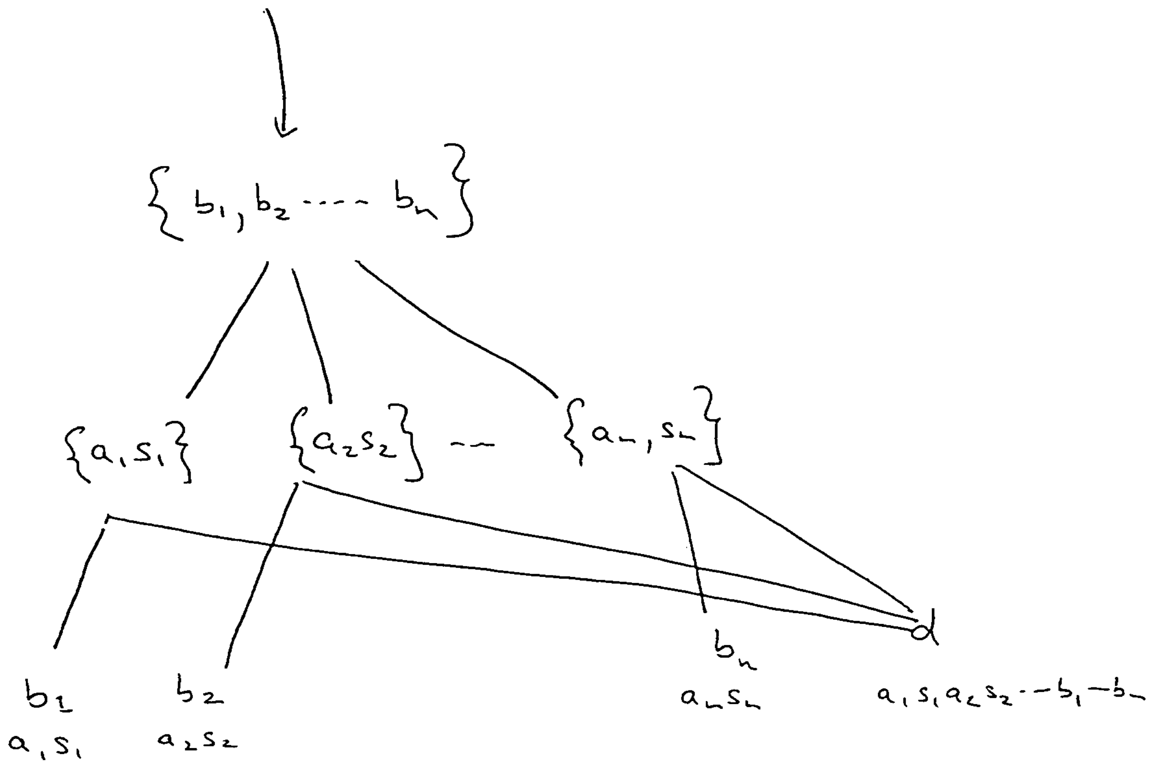

FIG 6